Amendments to the Specification

Please replace the paragraph at page 7, lines 27 through 29, and continuing on page 8, lines 1 through 10, with the following amended paragraph:

The present invention overcomes the high jitter of prior art data communication timing circuits by using a multiplying DLL with a low-offset, proportional phase comparator to eliminate both the dither and the 'last-cycle' mismatch. A block diagram of the present invention is shown in Figure 5. The improved multiplying DLL 147 generates bit clock 112 to sequence data multiplexer 102 and data demultiplexer 103. The use of a proportional phase comparator 147 overcomes the dither of prior art multiplying DLLs by eliminating the oscillation of the control voltage about its proper value. A very low-offset phase comparator that directly compares rclk to bclk eliminates the 'last-cycle' mismatch inherent in prior-art multiplying DLLs. The preferred embodiment uses a low-offset combined phase comparator and charge pump, as described in ~~pending~~ U.S. patent application 09/414,761 filed October 7, 1999, now U.S. Patent 6,275,072, issued August 14, 2001 to [[by]] Dally et al. for Combined Phase Comparator and Charge Pump Circuit, to realize both phase comparator 147 and charge pump 144.

Please replace the paragraph at page 8, lines 23 through 29, and continuing on page 9, lines 1 through 8, with the following amended paragraph:

Proportional phase comparator 147 directly compares the phase of reference clock rclk 111 and bit clock bclk 112 and generates signals up and down which are proportional to the amount of phase difference. These signals cause charge pump 144 to adjust the level of vctrl which in turn controls the delay of the delay line. In the preferred embodiment this is done by using the select signal 146 as a window signal to a combined phase comparator and charge pump of the type described in ~~pending~~ patent application 09/414,761, now U.S. Patent 6,275,072.. Signals rclk and bclk are only examined by the phase comparator when window signal sel 146 is high. When rclk rises before bclk during the timing window when sel is asserted, the delay line is too slow. Thus, the phase comparator causes signal up to be asserted when rclk=1, bclk=0,

and sel=1. This causes vctrl to be increased, speeding up the delay line and bringing rclk and bclk into alignment. Similarly, if bclk rises before rclk when sel is asserted , the delay line is too fast. To correct for this case, the phase comparator asserts signal down when rclk=0, bclk=1, and sel=1. This causes vctrl to be reduced, slowing the delay line and bringing rclk and bclk into alignment.